2. (New) The backplane as set forth in Claim 1 wherein said low tier that is capable of aggregate traffic rates of up to approximately two gigabits per second comprises:

a low tier bus comprising a switching architecture that (1) allows a circuit board card on an input side of a connection to transmit data to a circuit board card on an output side of said connection, and that (2) allows a circuit board card on an output side of a connection to receive data from a circuit board on an input side of said connection.

3. (New) The backplane as set forth in Claim 2 wherein said low tier bus supports one of: packet based traffic, unicast traffic, multicast traffic, and broadcast traffic.

4. (New) The backplane as set forth in Claim 2 wherein said low tier bus supports asynchronous transfer mode traffic.

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5. (New) The backplane as set forth in Claim 4 wherein said low tier bus wraps asynchronous transfer mode cells with a header to allow said low tier bus to switch cell based traffic according to a connection map on each circuit board card connected to said low tier bus.

6. (New) The backplane as set forth in Claim 2 wherein said low tier bus comprises two (2) parallel busses, each of which comprises a thirty two (32) bit data path.

7. (New) The backplane as set forth in Claim 2 wherein said low tier bus operates at a clock rate equal to one half of a clock rate of said backplane.

8. (New) The backplane as set forth in Claim 7 wherein said low tier bus clock rate is 32.768 MHz.

9. (New) The backplane as set forth in Claim 2 comprising a redundant clock reference for said low tier bus.

10. (New) For use in association with devices such as processors and modems used in wireless and wireline access systems, a backplane comprising:

a high tier that is capable of aggregate traffic rates of up to approximately twenty gigabits per second.

11. (New) The backplane as set forth in Claim 10 wherein said high tier that is capable of aggregate traffic rates of up to approximately twenty gigabits per second comprises:

a high tier bus; and

at least two switch matrix circuit board cards coupled to said high tier bus.

12. (New) The backplane as set forth in Claim 11 wherein said high tier bus comprises:

high speed serial links coupled to said at least two switch matrix circuit board cards and coupled to circuit board cards capable of sending and receiving high speed data traffic.

13. (New) The backplane as set forth in Claim 12 wherein said high speed serial links comprise:

point-to-point serial links comprising differential pairs for both a transmit path and a receive path.

14. (New) The backplane as set forth in Claim 13 wherein said high speed serial links operate at a clock rate equal to a clock rate of said backplane.

15. (New) The backplane as set forth in Claim 14 wherein said high speed serial link clock rate is 65.536 MHz.

16. (New) The backplane as set forth in Claim 14 comprising a high speed serial link serial/de-serial device that multiplies said high speed serial link clock rate by a factor of twenty (20), and wherein each high speed serial link is 8B/10B encoded.

17. (New) The backplane as set forth in Claim 12 comprising at least two (2) high speed serial links for each interface control processor slot in said backplane.

18. (New) The backplane as set forth in Claim 1 further comprising one of: a time division multiplex bus, a communications bus, a common control bus, and a Joint Test Access Group test bus.

19. (New) The backplane as set forth in Claim 18 further comprising at least one set of clock and framing resources.